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EXAMINER	
CHOW, CHARLES CHIANG	
ART UNIT	**PAPER NUMBER**
2685	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/036,831	GOLDMAN, STANLEY J.	
	Examiner	Art Unit	
	Charles Chow	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 and 14-16 is/are rejected.

7)☒ Claim(s) 13 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12/21/2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2; 21/21/2001.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Abstract

1. The abstract of the disclosure is objected to because the abstract is too long, near 200 words.

Correction is required. See MPEP§ 608.01(b).

Applicant is reminded of the proper language and format for an abstract of the disclosure. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.
The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Drawing

2. The drawings are objected to because the minor typo error for the label for 406 is "course" tune in Fig. 7, which needs to be corrected to "coarse" tune. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5-6, 8, 10, 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Birleson (US 6,163,684) in view of Fujii(Us 6,396,330B1).

Regarding **claim 1**, Birleson teaches a multi-loop frequency synthesizer (PLL2-22, PLL3-23, PLL4-24 in 20, Fig. 1-2, col. 3, line 30 to col. 5, line 47) comprising an input terminal

(reference input of 5.25 MHz to 20 and 123, Fig. 1) for receiving an input reference signal having a frequency fr (5.25 MHz).

Birleson teaches a fine tune phase locked loop (PLL4-24, Fig. 2) operably coupled to the input terminal (terminal connection for 2.625 MHz through 20 and reference 5.25 MHz divided by 2 in 123 Fig. 1) and driven by the input reference signal (5.25 MHz), wherein the fine tune phase locked loop is operably to output a fine tune signal having a frequency fr*p where p is an integer (fine tuned PLL4-24 having fine step of 62.5 KHz, col. 5, line 14, and a divider P of value of (6 or 7)*N in 233-234, for the equivalent claimed P from applicant. The output frequency of the fine loop PLL 24 is the reference 2.625 MHZ * P, and P is equal to (6 or 7) *N).

Birleson teaches a coarse tune phase locked loop (PLL3-23, Fig. 2) operably coupled to the input terminal (input terminal to 222, Fig. 2) and driven by the input reference signal (5.25 MHz), wherein the coarse tune phase locked loop is operable to output a coarse tune signal having a frequency fr*A (the coarse PLL3-23 tunes to high frequency 1128.75 MHz or low frequency 1034.25 MHz, having step of 94.5 MHz which is the difference between 1128,75 MHz and 1034.25 MHz. The coarse tuned PLL3-23 has output frequency of reference frequency 5.25 MHz multiplied by N, as shown in Fig. 2).

Birleson teaches a translation phase locked loop (PLL2-22) having a unity multiplication factor (PLL2 -22 is a unity frequency translation loop as shown in Fig. 2) driving by the fine tune signal (output of 230 from PLL4-24), comprising a mixer (mixer 212 in PLL2-22, Fig. 2, col. 5, lines 31-33), the mixer is coupled between the coarse tune (PLL3-23) and the translation PLL (PLL2-22), wherein the mixer combines the coarse tune signal (output of

220) and a divided down output signal of the fine tune phase locked loop (output of divider 230, divide by 42. The summing has the similar structure as applicant Fig. 8-9), and couples the mixed signal (output of mixer 212) into the translation phase locked loop (mixer output is coupled to phase comparator 214), whereby an output signal is generated with a frequency which is proportional to the linear sum of the coarse tune signal and the fine tune signal (output frequency fo at 210 of PLL2-22 is also at output of 211 for mixing with coarse tuned frequency f_{coarse} from coarse PLL3 to produce mixer output fo-f_{coarse}. The mixer's output frequency is equal to the output frequency f_{fine} of fine tune PLL4 at phase comparator 214. Thus, fo-f_{coarse}=f_{fine}, which is fo = f_{coarse}+f_{fine}, the linear sum of the coarse tuned and fine tuned frequencies), where by the low multiplication factor (the PLL2-22 is a translation loop which has unit multiplication factor without utilizing frequency divider) and high bandwidth (94.5 MHz) of the coarse tune loop and the unit multiplication factor of the translation loop reduces the phase noise of the frequency synthesizer (col. 5, lines 41-47, col. 1, lines 61-64, col. 2, lines 23-43, col. 4, lines 63-64).

Birleson does not clearly teach the Gilbert cell double balanced mixer. However, Fujii teaches the mixer circuit is for the Gilbert cell double balanced mixer with reduced (col. 1, lines 6-8, col. 4, lines 49-52). Fujii teaches an improved mixer circuit for Gibert cell double balance mixer, for reducing distortion (col. 4, lines 32-52). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Birleson, and to include Fujii's Gilbert cell double balanced mixer with reduced distortion, such that the mixer could reduce the output signal distortion.

Regarding **claim 2**, Birleson teaches the fine tune PLL(PLL4-24) includes a divide by D element (230) operable to receive the fine tune signal having a frequency fr.p [reference input 2.625 MHz* (6 or 7)*N, p is (6 or 7) *N] where D is an integer (42) and an output of divide by D element also comprising an output of the fine tune PLL and provides a signal frequency proportional to fr.P/D (reference input 2.625 Mhz * (6 or 7)* N/42. where p is (6 or 7)*N, D is 42, which is the fr*P/D)

Regarding **claim 3**, Birleson teaches the fine tune PLL (PLL4-24) includes a divide by Nr element (5.25MHz divide by 2 is 2.625 MHz, where 2 is the value for Nr) operable to receive the input reference signal having a frequency fr (5.25 MHz) and a divide by D element (42 in 230) operable to receive the fine tune signal having a frequency fr*p (output of VCO4, 231), and output of the divide by D element also comprising an output of fine tune PLL (output of 230) and provides a signal frequency proportional to fr*P/D*Nr (reference fr of value 5.25 MHz multiplied by p of value (6 or 7) *N, then, divide by D of value 42 and divide by Nr of value 2).

Regarding **claim 5**, Birleson teaches the D (value of 42) which is greater than Nr (value of 2). Bezzam taught above the A is less than P (col. 5, lines 42-43).

Regarding **claim 6**, Birleson teaches all the elements of the frequency synthesizer are on a single integrated circuit chip (the coarse and fine tuning are controlled substantially on a single monolithic circuit, col. 8, lines 4-6, col. 7, lines 53-60, col. 7, lines 16-21, col. 7, lines 43-44).

Regarding **claim 8**, Birleson teaches the fine tune and coarse tune PLLs (the fine tuned PLL4-24 and coarse tuned PLL3-23), a phase detector (235, 222) operably coupled to receive

the input reference signal (2.625 MHz, 5.25 MHz) having a frequency fr (5.25 MHz) and a divided down feedback signal (output of 234, 223) and to generate a phase detected signal (output of 235, 222). Birleson teaches a loop filter (323, Fig. 3, col. 5, line 66 to col. 6, lines 11-15) coupled to receive the phase detection signal (phase detector 32) and output a tune voltage (input voltage to VCO 33), an oscillator (VCO4, VCO3) operably coupled to receive the tune voltage and generate a signal frequency proportion to the tune voltage, a divider (233, 234, 223) operably coupled between an input of the phase detector (235, 222) and the oscillator output (VCO4, VSO 3) which is the phase locked loop output, and operable to generate the divided sown feedback signal, which is a lower frequency signal of the oscillator output.

Regarding **claim 10**, Birleson teaches a divide by D element (230) coupled between the fine tune output at 231 of PLL4-24) and the translation PLL (PLL2-22), a divide by Nr element (value of 2 in 123, Fig. 1) coupled between the input terminal and the fine tune PLL4-24.

Regarding **claim 14**, Birleson teaches a method of synthesizing a signal from a low frequency reference signal (5.25 MHz) comprising: inputting a reference with frequency fr (5.25 MHz) to an input terminal of the fine tune PLL4-24 and a coarse tune PLL3-23, multiplying a frequency fr of the reference signal by a factor P [(6 or 7)*N] in the fine tune PLL(PLL4-24) to generate a fine tune signal, multiplying a frequency fr by a factor A (N in 223) in the coarse tune PLL (PLL3-23) to generate a coarse tune signal, applying the fine tune signal (output of 230) to a translation PLL (PLL2-22) and a mixer (212) summing the coarse tune signal (output of 220) and a divided down output of fine tune signal(output of 230, The summing has the similar structure as applicant Fig. 8-9.) and coupling the mixed

signal into the translation PLL (PLL2-22) to generate an output signal having a higher frequency proportional to fr*(P/D*Nr+A) [the equation derivation is noted in Fig. 2 of Birleson for fo-fr*A=fr*P/(Nr*D), so output frequency is fo=fr*(P/(Nr*D) +A) for the proportion].

Birleson does not clearly teach the Gilbert cell double balanced mixer. However, Fujii teaches the mixer circuit is for the Gilbert cell double balanced mixer with reduced (col. 1, lines 6-8, col. 4, lines 49-52). Fujii teaches an improved mixer circuit for Gibert cell double balance mixer, for reducing distortion (col. 4, lines 32-52). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Birleson, and to include Fujii's Gilbert cell double balanced mixer with reduced distortion, such that the mixer could reduce the output signal distortion.

Regarding **claim 15**, Birleson teaches the dividing the reference signal by Nr (2.625 MHz = 5.25 MHz/Nr and Nr has value of 2), prior to applying the reference signal to the fine tune PLL (5.25 MHz to 123 to produce reference 2.625 Mhz for fine tune PLL4-24, Fig. 1-2), and dividing the fine tune signal by a factor D (230 of vale 42) prior to applying the fine tune signal (output of 230) to the translation loop PLL2-22.

4. Claims 4, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Birleson in view of Fujii, as applied to claim 3 above, and further in view of Bezzam et al. (US 6,115,586).

Regarding **claim 4**, Birleson and Fujii do not clearly teach P, A, D and NR are programmable. Bezzam et al. (Bezzam) teaches the frequency synthesizer wherein P, A, D and Nr are programmable (col. 5, lines 36-44), for a multiple loop radio frequency synthesizer (abstract, Fig. 506, summary of invention), having PLL 132, 138, 150, and SSB

mixer 146, Fig. 6, Fig. 5). Bezzam teaches the improved synthesizer technique of integrating three PLL onto a single chip for reducing the cost with minimized phase noise (col. 1, line 62 to col. 2, lines 11). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Birleson, and to include Bezzam's programmable dividers P, A, D, Nr, such that the multiple synthesizer could be integrated onto a single chip with low phase noise.

Regarding **claim 7,** Birleson teaches the translation PLL (PLL2-22) comprises a phase detector (214) coupled to receive the divided down fine tune signal (output of 230) and the mixer 212 output, and to output a phase detection signal (output of 214), a voltage controlled oscillator (VCO2, 210) coupled to receive the tune voltage output (213) and generate a signal frequency proportional to the tune voltage, a mixer coupled between the coarse tune and the translation phase locked loops (coarse PLL3-23, translation PLL2-22), the mixer (212) combines the coarse tuned signal (output of 220) and the divided down output signal (230) of the fine tune PLL4-24, and couples the mixed signal into the translation loop (PLL2-22), whereby an output signal is generated with a frequency which is proportional to the linear sum of the coarse tune signal and the fine tune signal (output frequency fo at 210 of PLL2-22 is also at output of 211 for mixing with coarse tuned frequency f_{coarse} from coarse PLL3 to produce mixer output fo-f_{coarse}. The mixer's output frequency is equal to the output frequency f_{fine} of fine tune PLL4 at phase comparator 214. Thus, fo-f_{coarse}=f_{fine}, which is fo = f_{coarse}+f_{fine}, the linear sum of the coarse tuned and fine tuned frequencies). Fujii taught above the Gilberst cell double balance mixer, Bezzam taught a low pass filter (63, col. 2, lines 62-63) coupled to receive the mixed signal output of the mixer (62) and to produce a filtered output signal

(Afl), a loop filter (178, Fig. 6) coupled to receive the phase detection signal and to output a tune voltage (output of 176).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Birleson in view of Fujii, as applied to claim 8 above, and further in view of Dujmenovic (US 2002/0118,308 A1).

Regarding **claim 9**, Birleson and Fujii do not clearly teach a dual modulus prescaler, a swallow divider, a programmable divide by np element.

Dujmenovic teaches the dual modulus prescaler (72, Fig. 3) operably coupled to receive the phase locked loop output (output of oscillator 70) wherein the dual modulus prescaler comprises a divide by P1 or P1+1 integers, and generates a divide by P1 or P1+1 result output from the operation of the elements ([0038-0045]), a swallow divider (76) coupled to the dual modulus prescaler (72) wherein the swallow divider (76) comprises a divide by ns element (programmable counter +A), where ns (programmable counter +A) is an integer and determines a modulation frequency M for the dual modulus prescaler (feedback from 76 to 72), and a programmable divide by np element (74) operably coupled to the output of the dual modulus prescaler (72), where np (N1) is an integer, and wherein the divide by np element is operably to divide the dual modulus prescaler output frequency by np (N1), whereby the divider provides a signal frequency proportional to (nm*np +ns) fref or (nm+1*np+ns). Dujmenovic teaches the similar dual modulus prescaler structure as applicant's dual modulus structure in Fig. 9 for 604, 606). Dujmenovic teaches the television tuner having improved fine frequency tuning preventing from interference, having multiple

synthesizers (62, 64, 66, Fig. 3) for integrated on a single integrated circuit substrate [0001, 0005-0012]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Birleson above, and to include Dujmenovic's dual modulus precaler 72, swallow divider 76, a programmable divider 74, for the synthesizer to be integrated onto a single substrate, such that frequency generated by the synthesizer could be fine tuned without interference.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Birleson in view of Fujii, as applied to claim 3 above, and further in view of Hirata et al. (US 5,353,311).

Regarding **claim 11**, Birleson does not clearly teach a frequency modulation circuit coupled to the fine tune phase locked loop whereby the frequency synthesizer outputs a narrow band FM filtered at the translation PLL, providing broader bandwidth into microwave frequency ranges.

Hirata teaches a frequency modulation circuit (DDS 1, Fig. 1, Fig. 6) for generating frequency hopping FM signal from DDS1 to first phase locked loop via S3 (Fig. 1, col. 2, line 56 to col. 3, line 57), and phase locked oscillator 2 has sufficiently narrow loop band to remove spurious signal from the hopping signal S3 (col. 3, lines 52-57). The phase locked oscillator 3, second phase locked oscillator, has loop band for suppressing phase noise of the phase modulated signal ascribable to the VCO (abstract). Hirata teaches the modulated signal by utilizing frequency modulation circuit DDS 1 and PLL 2, 3 with reduced spurious signal and phase noise (col. 1, lines 30-60). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Birleson above, and to include

Hirata's frequency modulation circuit for synthesizer, such that the modulated signal could have reduced spurious signal and phase noise.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Birleson in view of Fujii, Bezzam, as applied to claim 7 above, and further in view of Caulfield et al. (US 5,757,867).

Regarding **claim 12**, Birleson, Fujii, Bezzam do not clearly teach the sigma-delta modulation smoothing technique for the low pass filter coupled to the Gilbert cell double balanced mixer, although Fujii taught the Gilbert cell double balance mixer.

Caulfield et al. (Caulfield) teaches the sigma delta modulator 100 (Fig. 1) connected to mixer 12 having low pass filter 14 for sigma delta modulation smoothing filtering technique (abstract, col. 4, lines 26-54). Caulfield teaches the low pass filter for receiving mixer output signal for producing high resolution signal (col. 1, line 53 to col. 2, lines 14). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Birleson above, and to include Caulfield 's low pass filtering for smoothing sigma-delta modulation, such that output signal from mixer output could be filtered to provide high resolution signal.

Claim Objection

9. Claim 13, 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding **claim 13**, Birleson and Fuji discloses the method of claim 1. Birleson and Fuji fails to further disclose a first lock detector coupled to the fine phase locked loop, a second lock detector coupled to the coarse tune phase locked loop, an AND gate coupled to receive the output of the first and second lock detectors, and a sweep circuit, wherein when a lock condition is detected in both the first and second lock detector, the sweep signal is initiated which generates a frequency sweep of the translation loop VOC to establish a translation loop lock condition.

Regarding **claim 16**, Birleson and Fuji discloses the method of claim 1. Birleson and Fuji fails to disclose a lock detection, the applying of the fine tune loop phase detector inputs to a fine tune lock detector circuit, the applying of the coarse tune loop detector inputs to a coarse tune lock detector circuit, a sweep operation, the applying one-shot circuit generate a pulse to initiate a sweep circuit associated with a loop filter of the translation loop, generating a ramp waveform within the sweep circuit, applying the sweep ramp waveform to a VCO of the translation loop, although Keelty (US 4,072,905 in below) teaches the AND gate (Fig. 5) for detecting the lock of PLL1 (30) and PLL2 (32) for initiating the stopping of the scanning in synthesizer 36 (col. 2, lines 37-57), applying the PLL30 detector circuit (LD in 30, Fig. 5, col. 2, lines 10-56), and PLL32 lock detector circuit (LD in 32), applying both detector circuit outputs to an AND gate (22 in Fig. 1, AND gate in Fig. 5), logically AND both lock detector outputs to indicate when both have achieved lock, to stop scanning in synthesizer 36 when both PLL1 and PLL2 are locked.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

A. (US 4,072,905), February 1978, Keelty teaches the AND gate (Fig. 5) for detecting the lock of PLL1 (30) and PLL2 (32) for initiating the stopping of the scanning in synthesizer 36 (col. 2, lines 37-57), applying the PLL30 detector circuit (LD in 30, Fig. 5, col. 2, lines 10-56), and PLL32 lock detector circuit (LD in 32), applying both detector circuit outputs to an AND gate (22 in Fig. 1, AND gate in Fig. 5), logically AND both lock detector outputs to indicate when both have achieved lock, to stop scanning in synthesizer 36 when both PLL1 and PLL2 are locked.

B. US 4,528,522), July 1985, Matsuura teaches an improved frequency synthesizer for FM transceiver having phase locked loop PLL 1 and PLL 2 (Fig. 3) with mixer 31 (Fig. 3).

C. US 5,015,971, May 1991, Taylor et al. teaches the synthesizer for generating frequency agile microwave signal having the sweep generator 98 (Fig. 1).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles Chow whose telephone number is (703)-306-5615.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban, can be reached at (703)-305-4385.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 872-9306 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Charles Chow C.C.

April 8, 2004.

4/19/04

QUOCHIEN B. VUONG
PRIMARY EXAMINER